Philadelphia University
Course Outline

Course Syllabus	
Course Title	Logic Circuits
Course Number	630211
Course Level	2nd year
Class Time	09:45 – 11:15(M-W)
Instructor	Dr. Qadri Hamarsheh
email	qhamarsheh@philadelphia.edu.jo
website	www.philadelphia.edu.jo/academics/qhamarsheh
Prerequisites	0761099
Office Hours	Hours: 10:10-11:10(Sun-Tue-Thu), Office 712
Text Book	Digital Fundamentals, Thomas L. Floyd 10th ed., Pearson International Edition, 2009.

Course Goals:

The goal of the course is to Provide students with an introduction to the analysis and design of combinational and sequential digital logic circuits.

Time Schedule:

Duration: 16 weeks **Lectures:** 3 hours /week
Tutorial: None **Laboratories:** 3 hours/ week (630266)

Objectives:

At Completing this module the student should be able to :

1- Provide the student design methodologies for electronic circuits, to use mathematical expressions to describe the functions of simple combinational and sequential circuits.
2- Provide student with the approaches to converting numerical data from one format to another, to use different formats to represent numerical data.
3- Study Boolean algebra, basic laws and rules in logic design, DeMorgan's theorem, Karnaugh map, and approaches to simplifying logic circuits.
4- Study systematical design methodology for combinational logic circuits and build this kind of digital systems by using some IC devices.
5- Study systematical design methodology for sequential logic circuits.

Course Contents

		Week
❖	NUMBERS SYSTEMS AND CODES	1
❖	LOGIC SIGNALS ANS GATES	2
❖	COMBINATIONAL CIRCUIT ANALYSIS, (CIRCUIT MINIMIZATION, KARNAUGH MAPS.	2
❖	COMBINATIONAL LOGIC DESIGN PRACTICES, (DECODERS, ENCODERS, MUXS, AND DMUXS, ADDERS, SUBTRACTORS AND MULTIPLIERS).	3
❖	SEQUENTIAL LOGIC DESIGN PRINCIPLES: - LATCHES, SR FLIP-FLOP, JK FLIP-FLOP, AND D FLIP-FLOP - MASTER-SLAVE FLIP-FLOP, AND TRIGGERED FLIP-FLOPS	3
❖	SEQUENTIAL LOGIC DESIGN PRINCIPLES: (REGISTERS, SHIFT REGISTERS, AND COUNTERS)	3

Mode of Assessment

1- First Exam 20%
2- Second Exam 20%
3- Quizzes\Homework\ and or Projects 20%
4- Final Exam 40%

References

1- Introduction to Logic Design, Alan B. Marcovitz, Third Edition, McGraw-Hill, 2010.
2- Logic and computer design fundamentals, M. Morris Mano, Charles R. Kime , Pearson Prentice Hall, 4th ed., 2008
3- Digital Design, 4th Edition, M. Morris Mano and Michael D. Ciletti, Prentice Hall, 2007.
4- Digital Electronics: Principles and Applications, R. L. Tokheim, 5th Edition, McGraw-Hill, 2000.
5- Practical Digital Logic Design and Testing, P. K. Lala, Prentice Hall, 1996.
6- Introduction to Digital Logic Design, J. P. Hayes, Addison-Wesley, 1996.